

**METHODS, APPARATUS AND COMPUTER PROGRAM PRODUCTS FOR  
GENERATING SELECTIVE NETLISTS THAT INCLUDE  
INTERCONNECTION INFLUENCES AT PRE-LAYOUT AND POST-  
LAYOUT DESIGN STAGES**

**ABSTRACT OF THE DISCLOSURE**

Operations for generating an integrated circuit netlist include generating a first schematic of an integrated circuit having a plurality of cells therein and generating a second schematic that defines pre-layout electrical interconnects between the plurality of cells of the integrated circuit and approximates parasitic resistances and parasitic capacitances of the pre-layout interconnects. The first and second schematics are then combined at corresponding first and second ports within the first and second schematics, respectively. Operations also include generating an integrated circuit netlist by generating a circuit schematic that defines post-layout electrical interconnects between the plurality of cells of the integrated circuit and approximates parasitic resistances and parasitic capacitances of the post-layout interconnects. This circuit schematic is then combined with the first schematic at corresponding first and second ports therein. These embodiments may also be configured to generate a layout schematic from the first schematic of the integrated circuit and generate parasitic resistances and capacitances of the post-layout interconnects that extend between a plurality of cells in the layout schematic. Operations are then performed to generate parasitic resistances and capacitances of interconnects internal to at least one cell in the layout schematic.